This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

OIPE JC12
JUL 16 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 12, 2004
(Date of Deposit)

Harold C. Moore
Name of person mailing Document or Fee

Signature

July 12, 2004
Date of Signature

Re:		
	Application of:	Slater et al.
	Serial No.:	09/828,701
	Filed:	April 6, 2001
	For:	Electronic Meter Having Random Access Memory with Passive Nonvolatility
	Group Art Unit:	2829
	Examiner:	E. Karlsen
	Our Docket No.:	1505-0099

TRANSMITTAL OF BRIEF ON APPEAL

Please find for filing in connection with the above patent application the following documents:

1. Original of the Appeal Brief;
2. Three (3) copies of the Appeal Brief;
3. A Check in the amount of $330.00; and
4. One (1) return post card.

The due date for filing a Brief on Appeal fell on Saturday, July 10, 2004. Therefore, this Brief on Appeal is being timely filed on Monday, July 12, 2004. Enclosed please find a check in the amount of $330.00 to cover the filing fee of an Appeal Brief as required by 37 C.F.R. § 1.17(e). Please charge any deficiency, or credit any overpayment to Deposit Account No. 13-0014.

Respectfully Submitted,

MAGINOT, MOORE & BECK, LLP

July 12, 2004

Harold C. Moore
Registration No. 37,892
Bank One Center/Tower
111 Monument Circle, Suite 3000
Indianapolis, IN 46204-5115

Enclosures

OIPE
JUL 16 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 12, 2004
(Date of Deposit)

Harold C. Moore
Name of person mailing Document or Fee

Signature

July 12, 2004
Date of Signature

Re:	Application of:	Slater et al.
	Serial No.:	09/828,701
	Filed:	April 6, 2001
	For:	Electronic Meter Having Random Access Memory with Passive Nonvolatility
	Group Art Unit:	2829
	Examiner:	E. Karlsen
	Our Docket No.:	1505-0099

BRIEF ON APPEAL

Sir:

This is an appeal under 37 CFR § 1.191 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the final rejection of claims 1-11, 20 and 21 of the above-identified patent application. These claims were indicated as finally rejected in an Office Action dated February 10, 2004. Three copies of the brief are filed herewith. A check in the amount of **$330.00** is provided herewith to cover the fee required under 37 CFR § 1.17(f). Also, please provide any extension of

07/16/2004 EFLORES 00000130 09828701
01 FC:1402 330.00 OP

time which may be necessary and charge any fees which may be due to Deposit Account No. 13-0014, but not to include any payment of issue fees.

(1) REAL PARTY IN INTEREST

Landis+Gyr Inc. is the owner of this patent application, and therefore the real party in interest.

(2) RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to this patent application.

(3) STATUS OF CLAIMS

Claims 1-11, 20 and 21 are pending in the application. Claims 12-19 have been withdrawn from consideration.

Claims 1-11, 20 and 21 stand rejected and form the subject matter of this appeal. Claims 1-11, 20 and 21 are shown in the Appendix attached to this Appeal Brief.

(4) STATUS OF AMENDMENTS

Applicants filed a Response to Office Action dated November 3, 2003 ("Response") responsive to an Office Action dated August 1, 2003. A final Office Action dated February 10, 2004 was designated by the Examiner to be responsive to the Response.

(5) SUMMARY OF THE INVENTION

The present invention is directed to an arrangement for generating and storing metering information in a meter that measures a consumed commodity. A consumed commodity may be electrical energy, gas, or water by way of example. (See, e.g., Application at p.6). The arrangement includes a processing circuit and a non-volatile, rewriteable random access memory. Non-limiting examples of a processing circuit and non-volatile rewriteable random access memory are described in the Application at pages 7-9. The processing circuit is operable to generate metering information. Metering information may include real energy information, RMS voltage and/or current levels, power factor, volt-amp information, among other things. (See, e.g. *id.* at page 9, lines 1-2). The non-volatile, rewriteable random access memory stores metering information during normal operation, and is operable to retain the stored metering information in the absence of external electrical power. (See, e.g., *id.* at p.7, line 18 to p.8, line 1).

Nonvolatile random access memories do not have certain limitations of EEPROM, as is described at length in the specification, when incorporated as claimed.

In some additional embodiments, the non-volatile rewriteable random access memory stores program code to be executed by the processing circuit as well as the generated metering information. (See, e.g., *id.* at p.8, lines 15-19) In other embodiments, the processing circuit also generates metering information in the form of load profiling information that is also stored in the non-volatile rewriteable random access memory. (See, e.g., *id.* at p.8, lines 10-17). In still other embodiments, the non-volatile rewriteable random access memory is furthermore used for interim calculation values. (See, e.g. *id* at page 21, lines 10-19, claim 8).

(6) ISSUES

Whether claims 1-11, 20 and 21 are unpatentable under 35 U.S.C. § 112, second paragraph as being indefinite.

Whether claims 1-11, 20 and 21 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,564,159 to Lavoie et al. (hereinafter "Lavoie").

Whether claims 1-11, 20 and 21 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,429,785 to Griffin et al. (hereinafter "Griffin").

Whether claims 1-11, 20 and 21 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,351,223 to DeWeerd et al. (hereinafter "De Weerd").

Whether claims 1-11, 20 and 21 are unpatentable under 35 U.S.C. § 103(a) as being obvious over U.S. Patent no. 5,548,527 to Hemminger et al. (hereinafter Hemminger).

(7) GROUPING OF CLAIMS

The claims do not all stand or fall together.

Claims 1, 3-7, 9, 11 and 21 form a first separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claims 2 and 20 form a second separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claims 8 forms a third separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claims 10 forms a fourth separately patentable group which is argued

independently of the other claims for purposes of this appeal.

(8) ARGUMENT

First Claim Grouping: **Claims 1, 3-7, 9, 11 and 21 are Not Indefinite, Anticipated, nor Obvious**

Discussion re: Patentability of Claim 1

1. Claim

Claim 1 is directed to an arrangement for generating and storing metering information in a meter that measures a consumed commodity. The arrangement includes a processing circuit and a non-volatile, rewriteable random access memory.

2. The Examiner's Indefiniteness Rejection

The Examiner rejected claim 1 as allegedly being indefinite. It is submitted that claim 1 sufficiently particularly points out and distinctly claims the subject matter which applicant regards as the invention. However, claims 1, 20 and 21 appear to have an inadvertent typographical error, using the word "rewriteably" instead of "rewriteable". Applicants will amend the claims to correct this inadvertent, minor typographical error upon a determination of allowability of the claims over the prior art. Accordingly, to the extent the Examiner would remove the indefiniteness rejection if the word "rewriteably" was replaced by "rewriteable", applicants do not appeal this indefiniteness rejection.

Nevertheless, as will be discussed below, the Examiner does not appear to base the indefiniteness rejection on these grounds. To the extent the Examiner alleges that

claim 1 is invalid due to indefiniteness regardless of whether the term "rewriteably" were replaced by the term "rewriteable", the Applicants appeal the indefiniteness rejection.

In particular, the Examiner set forth the following reasoning for the anticipation rejection.

> The exact meaning of "non-volatile, [rewriteable] random access memory" is not clear. Applicants have cited a dictionary meaning and argue that flash memory is not ramdom access memory because is can only be erased in blocks and not in single byte increments. A byte is a block of bits and it would appear that the difference is only a matter of size of the blocks. A flash memory can be randomly accessed a block at a time which in a broad sense is a random access memory.

(Final Office Action at p.2). Applicants respectfully submit that the above quoted argument does not make out a prima facie case of indefiniteness under 35 U.S.C. §112, second paragraph. The fact that the Examiner believes "that the difference [between random access memory and flash memory] is only a matter of the size of the blocks" does not make the phrase "random access memory" somehow indefinite.

The phrase "random access memory" is used ubiquitously in the relevant art to describe a certain type of memory. Similarly, the phrase "flash memory" is also used universally in the relevant art to describe another type of memory. As opposed to random access memory, a flash memory must be erased in large sectors, i.e., several bytes. Those of ordinary skill in the art can distinguish between a flash memory and a random access memory based on the granularity with which random access memory may be rewritten.

Such a difference is further outlines in a technical dictionary coupled to the Applicants Response to Office Action dated November 3, 2003. The Examiner admits the difference, yet bases an indefiniteness rejection on application of a broader meaning to random access memory than is accepted by the relevant technical community and indeed the general populace.

It is respectfully submitted that the claim term is sufficiently definite. A "non-volatile, rewriteable random access memory" is a *random access memory*, as that phrase is normally used, that incorporates technology that makes the memory non-volatile. Several examples are now known in the art, including ferromagnetic RAM, and ferro-electric RAM.

For the above reasons, it is respectfully submitted that the Examiner's indefiniteness rejection of claim 1 should be reversed.

3. The Examiner's Anticipation Rejection Should be Reversed

The Examiner rejected claim 1 as allegedly being anticipated by Lavoie, Griffin and DeWeerd. The Examiner's rejection of claim 1 over these references should be reversed for two reasons. First, the Examiner has tacitly admitted that claim 1 is patentable over Lavoie, Griffin and DeWeerd in the Final Office Action. Second, the Lavoie, Griffin and DeWeerd fail to disclose or suggest a nonvolatile random access memory as claimed in claim 1.

A. The Examiner Alleged that Applicants' Amendments Necessitated New Grounds of Rejection

In the Final Office Action, the Examiner alleged that Applicant's amendment (Response to Office Action dated November 3, 2003) necessitated new ground(s) of rejection presented in the Final Office Action. (P.4). However, the Examiner appears to have maintained, in the Final Office Action, the exact same rejection as that responded to in the November 3, 2003 response. This cannot be. If the Examiner maintains that original grounds for rejection presented in the Examiner's August 1, 2003 Office Action

were sufficient to establish a prima facie case of anticipation, then no "new ground(s)" for rejection would be *necessitated.*

In particular, in the August 1, 2003 office action, the Examiner rejected claims 1-11, 20 and 21 as being anticipated by Lavoie, Griffin and DeWeerd, citing particular columns of each patent as disclosing the claimed subject matter. (August 1, 2003 office action at pp.2-3). The Applicant traversed the rejection in the Response to Office Action dated November 3, 2003, arguing that a "flash memory" (present in Lavoie, Griffin and DeWeerd) is not a "random access memory". The Applicant further amended the independent claims to further clarify that "nonvolatile" meant that the memory retained its contents in the absence of any power source external to the memory itself. (November 3, 2003 Response to Office Action at pp.2&8).

Thereafter, in the Final Office Action, the Examiner repeated the anticipation rejection of the claims over Lavoie, Griffin and DeWeerd *without any modification.* (Final Office Action at pp.2-3). Yet, the Examiner stated that applicants' November 3, 2003 amendment "necessitated new ground(s) of rejection". As discussed above, if the Examiner was maintaining his original rejection with respect to Lavoie, Griffin and DeWeerd, then no new grounds would be necessitated.

For this reason as well as the substantive reasons discussed below, it is respectfully submitted that anticipation rejection of claim 1 as being anticipated by Lavoie, Griffin and DeWeerd should be reversed.

B. Lavoie Does Not Teach a Nonvolatile RAM as Claimed

Lavoie fails to teach, show or suggest "a non-volatile, rewriteable random access memory", as called for in claim 1. In particular, Lavoie teaches the use of a *flash* memory as the nonvolatile memory. It appears that the Examiner is alleging that the flash memory of Lavoie constitutes the claimed nonvolatile random access memory (See August 1, 2003 office action at p.2; Final Office Action at pp.2-3). However, a flash memory is *not* a random access memory.

Flash memory, as is known in the art and as admitted by Lavoie, is a type of non-volatile memory in which large sectors of memory are written by "flashing" the sectors to erase any existing material, and then writing data to the sector. As noted by Lavoie:

> Flash memory 118 is typically organized into multiple large sectors (64 KB) which can be erased in their entirety. When flash memory is erased, all bits in in a sector are set to 1. When data is written, 1 bits are changed to 0 bits. *Once a bit has been changed to a 0, it cannot be changed back to a 1 without erasing the entire sector.*

(Lavoie at col. 10, lines 62-67) (emphasis added). Similarly, the Microsoft Computer Dictionary provides the following definition of "flash memory"

> A type of nonvolatile memory. Flash memory is similar to EEPROM memory in function but it must be erased in blocks, whereas EEPROM can be erased one byte at a time. Because of its block-oriented nature, flash memory is commonly used as a supplement to or replacement for hard disks in portable computers. . . . *A disadvantage of the block-oriented nature of flash memory is that it cannot be practically used as main memory (RAM) because a computer needs to be able to write to memory in single-byte increments.*

(Microsoft Computer Dictionary, Fourth Edition, Microsoft Press, 1999 at p.188, see Exh. A) (emphasis added).

Thus, the sources described above clearly recognize the distinction between block addressable flash memory and RAM. A flash memory is only block rewriteable, while random access memory may be rewritten in smaller increments. The present invention clearly claims a non-volatile *random access memory.*

Because Lavoie employs a flash nonvolatile memory, Lavoie fails to teach or suggest "a non-volatile, rewriteable random access memory" as called for in claim 1. As a consequence, it is respectfully submitted that the rejection of claim 1 as being anticipated by Lavoie is in error and should be reversed.

C. The Applicant's Provisional Application Pre-Dates Lavoie's Non-Provisional Filing Date

Independent of those reasons discussed above, the Examiner has not made a prima facie case of anticipation with respect to Lavoie. In particular, claim 1 stands rejected as allegedly being anticipated by Lavoie under 35 U.S.C. 102(e). In particular, the Examiner relies on columns 8-11 of Lavoie. However, Lavoie has a non-provisional filing date of June 29, 2000, while applicant has a priority date of April 7, 2000 for the subject matter of the claims.

Applicant appreciates that Lavoie claims priority to an earlier provisional application serial no. 60/141,771, filed June 30, 1999. Applicant has not seen U.S. Provisional Patent Application Serial No. 60/141,771 and cannot comment as to how much that document differs from Lavoie. However, the Examiner has not established that the portions (cols. 8-11) of Lavoie upon which the rejection of claims 1-11, 20 and 21 were present in the provisional application serial no. 60/141,771. Accordingly, the Examiner has failed to set forth a prima facie case of anticipation under 35 U.S.C. 102(e).

D. Griffin Does Not Teach a Nonvolatile RAM as Claimed

Griffin fails to teach, show or suggest "a non-volatile, rewriteable random access memory", as called for in claims 1, 20 and 21.. Griffin, like Lavoie, teaches the use of a

flash memory as the non-volatile memory. The Examiner contends that the flash memory of Griffin constitutes the nonvolatile random access memory (See August 1, 2003 office action at p.2; Final Office Action at pp.2-3). As discussed above, a flash memory is not a random access memory.

Griffin also mentions the use of non-volatile RAM. However, Griffin uses this term to describe *battery-backed* RAM.. (Griffin at col. 8, lines 53-58). As discussed in the present application, battery-backed RAM poses issues and difficulties which the claimed invention was intended to overcome. (Application at pp. 4-5). The claimed invention is clearly distinguished from battery-backed RAM, because, as claimed, the "non-volatile, rewritable random access memory [is] operable to retain the stored metering information in the absence of electrical power from a source external to the non-volatile, rewriteably random access memory." In other words, the *claimed* non-volatile RAM stores information even without a battery back-up.

For all of the foregoing reasons, it is respectfully submitted that Griffin fails to teach or suggest all of the elements of claim 1. As a consequence, the anticipation rejection of claim 1 over Griffin is in error and should be reversed.

E. DeWeerd Does Not Teach a Nonvolatile RAM as Claimed

DeWeerd similarly fails to teach, show or suggest "a non-volatile, rewriteable random access memory", as called for in claim 1. DeWeerd, like Lavoie and Griffin, teaches the use of a *flash* memory as the nonvolatile memory. As discussed above, a flash memory is not a random access memory.

Accordingly, it is respectfully submitted that DeWeerd fails to teach or suggest all of the elements of claim 1. As a consequence, the anticipation rejection of claim 1 over DeWeerd is in error and should be reversed.

4. The Obviousness Rejection Should be Reversed

The Examiner has rejected claim 1 as allegedly being obvious over Hemminger. In particular, the Examiner alleged that it would have been obvious to replace the EEPROM of Hemminger with a non-volatile RAM. The Examiner has not set forth a legally sufficient motivation or suggestion to modify Hemminger as proposed.

The motivation to substitute a non-volatile RAM for the EEPROM of Hemminger as proposed by the Examiner is allegedly "because one of ordinary skill in the art would realize that so doing would enable faster writing to the non-volatile device with greater cycling capability."

Hemminger, however, does not appear to disclose a device that would benefit from "faster writing" or "greater cycling capability", and nothing in the prior art suggests that but for those advantages, the substitution of non-volatile RAM for EEPROM is otherwise a substitution of equals.

In particular, Hemminger does not employ an EEPROM in such a manner as to require "faster writing" and "greater cycling capability". Hemminger teaches a system that integrates EEPROM for storing data that is *infrequently* accessed, and instead integrates volatile program and data RAM for frequent storage or frequently changing data. (See e.g. Hemminger at col. 6, line 60 to col. 7, line 18; col. 11, line 62 to col. 12, line 19). The volatile RAMs are integrated into a large integrated circuit package. (*Id.* at

col. 6, lines 62-64 and Fig. 1).

Because the EEPROM is relatively infrequently accessed, the EEPROM of Hemminger does not require a large number of writing cycles, and certainly does not appear to require writing capabilities faster than that capable with standard EEPROM technology. Thus, it is not at all clear that the operation of Hemminger would be improved in any way by replacing the EEPROM with a non-volatile RAM such as a ferromagnetic RAM or the like.

In addition, because EEPROM technology was more mature than non-volatile RAM technologies such as ferromagnetic RAM or FRAM at the time the invention was made, greater cost and risk would be likely result using the latter. The prior art contains no motivation to assume such cost and risk in the device of Hemminger.

There can be no motivation or suggestion to modify a device to solve a problem that does not exist, or to improve a parameter that does not benefit the final product. Nothing in Hemminger suggests that greater write speed or greater cycling capability would improve Hemminger. Accordingly, the fact that non-volatile RAM provides faster writing and greater cycling capability does not provide a motivation or suggestion to modify Hemminger to incorporate a different, less established technology. For at least these reasons, it is respectfully submitted that the obviousness rejection of claim 1 is in error and should be reversed.

Discussion re: Patentability of Claims 3-7, 9 and 11

Claims 3-7, 9 and 11 all stand rejected on the same grounds as those applied to claim 1. Claims 3-7, 9 and 11 all both depend from and incorporate all of the limitations

of claim 1. Accordingly, for at least the same reasons as those set forth above in connection with claim 1, it is submitted that the indefiniteness, anticipation, and obviousness rejections of claims 3-7, 9 and 11 should be reversed.

Discussion re: Patentability of Claim 21

Claim 21 stands rejected on the same grounds as those applied to claim 1. Claim 21, like claim 1, includes a limitation directed to a nonvolatile, rewriteable random access memory. Substantially all of the reasons for reversing the anticipation, indefiniteness and obviousness rejections of claim 1 set forth above apply equally to claim 21.

Second Claim Grouping: Claims 2 and 20 are Not Indefinite, Not Anticipated, Nor Obvious

Discussion re: Patentability of Claim 2

1. Claim 2

As an initial matter, claim 2 depends from and incorporates all the limitations of claim 1. Accordingly, claim 2 is not indefinite and is furthermore patentable over the prior art for at least the same reasons as those set forth above in connection with claim 1.

2. Additional Limitations of Claims 2

Claims 2 also recites the following limitations:

> wherein the non-volatile rewriteable random access memory is further operable to store the load profiling information.

Thus, in contrast to claim 1, claim 2 further recites the nonvolatile rewriteable random access memory is operable to store load profiling information. Load profiling

information is known in the metering art is information that tracks usage over a number of time periods.

2. Claim 2 is Patentable Over Hemminger for Additional Reasons

In addition to the reasons set forth above in connection with claim 1, claim 2 is patentable over Hemminger because the proposed modification of Hemminger does not arrive at the invention of claim 2.

As discussed above, the Examiner alleges that it would have been obvious to modify Hemminger to substitute the EEPROM of Hemminger with a non-volatile RAM. Even if such a modification were made to Hemminger, the resulting device would not store load profiling information in the nonvolatile RAM.

Nowhere does Hemminger teach that load profiling information is stored in the EEPROM. Moreover, the Examiner does not specifically allege that Hemminger teaches storing load profiling information in the EEPROM. Thus, even if the EEPROM of Hemminger were replaced by a nonvolatile RAM, the nonvolatile RAM would not store load profiling information.

Accordingly, for at least this reason in addition to those set forth above in connection with claim 1, it is respectfully submitted that the obviousness rejection of claim 2 is in error and should be reversed.

Discussion re: Patentability of Claim 20

Claim 20 stands rejected on the same grounds as those applied to claim 1. Claim 20 is an independent claim that, like claim 1, includes a limitation directed to a

nonvolatile, rewriteable random access memory. Substantially all of the reasons for reversing the anticipation, indefiniteness and obviousness rejections of claim 1 set forth above apply equally to claim 20.

In addition, like claim 2, claim 20 includes a limitation directed to storing load profiling information in the nonvolatile random access memory. In particular, claim 20 recites storing metering information in the nonvolatile random access memory, and further recites that the metering information includes load profiling information. As discussed above in connection with claim 2, the modification of Hemminger proposed by the Examiner does not arrive at a device that stores load profiling information in a nonvolatile RAM. Accordingly, similar to claim 2, claim 20 is patentable over Hemminger for reasons independent of those discussed above in connection with claim 1.

Third Claim Grouping: Claim 8 is Not Indefinite, Not Anticipated, Nor Obvious

Discussion re: Patentability of Claim 8

1. Claim 8

As an initial matter, claim 8 depends from and incorporates all the limitations of claim 1. Accordingly, claim 8 is not indefinite and is furthermore patentable over the prior art for at least the same reasons as those set forth above in connection with claim 1.

2. Additional Limitations of Claims 8

Claim 8 also recites the following limitations:

> wherein the non-volatile rewriteable random access memory stores at least one interim metering variable generated by the processing circuit and subsequently retrieved by the processing circuit for calculation of a metering value.

Thus, in contrast to claim 1, claim 8 further recites the nonvolatile, rewriteable random access memory is operable to store at least one interim metering variable generated by the processing circuit and subsequently retrieved by the processing circuit for calculation of a metering value. In other words, the non-volatile rewriteable random access memory may further be used a scratchpad memory used by the processor to store interim metering variables.

2. Claim 8 is Patentable Over Hemminger for Additional Reasons

In addition to the reasons set forth above in connection with claim 1, claim 8 is patentable over Hemminger because the proposed modification of Hemminger does not arrive at the invention of claim 8.

As discussed above, the Examiner alleged that it would have been obvious to modify Hemminger to substitute the EEPROM of Hemminger with a nonvolatile RAM. Even if such a modification were made to Hemminger, the resulting device would not store interim values in nonvolatile RAM, wherein the interim values are generated by the processing circuit and are used subsequently by the processing circuit.

Hemminger does not appear to store such interim values in EEPROM. Moreover, the Examiner has not identified any portion of Hemminger in which Hemminger teaches storing interim values in the EEPROM. Thus, even if the EEPROM of Hemminger were replaced by a nonvolatile RAM, the nonvolatile RAM would not store interim values as

claimed in claim 8.

Accordingly, for at least this reason in addition to those set forth above in connection with claim 1, it is respectfully submitted that the rejection of claim 8 is in error.

Fourth Claim Grouping: Claim 10 is Not Indefinite, Not Anticipated, Nor Obvious

Discussion re: Patentability of Claim 10

1. Claim 10

As an initial matter, claim 10 depends from and incorporates all the limitations of claim 1. Accordingly, claim 10 is not indefinite and is furthermore patentable over the prior art for at least the same reasons as those set forth above in connection with claim 1.

2. Additional Limitations of Claim 10

Claim 10 also recites the following limitations:

> the processing circuit is operable to generate statistical commodity consumption information, said statistical commodity consumption information including commodity usage information for a plurality of time periods
>
> wherein the non-volatile rewriteable random access memory is further operable to store the statistical commodity consumption information.

Thus, in contrast to claim 1, claim 10 further recites the nonvolatile rewriteable random access memory is operable to store statistical commodity consumption information that includes commodity usage information for a plurality of time periods.

2. Claim 10 is Patentable Over Hemminger for Additional Reasons

In addition to the reasons set forth above in connection with claim 1, claim 10 is patentable over Hemminger because the proposed modification of Hemminger does not arrive at the invention of claim 10.

As discussed above, the Examiner alleged that it would have been obvious to modify Hemminger to substitute the EEPROM of Hemminger with a nonvolatile RAM. Even if such a modification were made to Hemminger, the resulting device would not store statistical commodity consumption information in nonvolatile RAM.

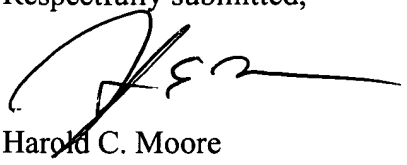
The Examiner does not specifically allege the portions of Hemminger that teach storing statistical commodity consumption information as claimed in the EEPROM. Applicant's attorney has reviewed Hemminger and has found no such teaching. Thus, even if the EEPROM of Hemminger were replaced by a nonvolatile RAM, the nonvolatile RAM would not store statistical commodity consumption information as claimed in claim 10.

Accordingly, for at least this reason in addition to those set forth above in connection with claim 1, it is respectfully submitted that the rejection of claim 10 is in error and should be reversed.

(9) CONCLUSION

For all of the foregoing reasons, claims 1-11, 20 and 21 are not unpatentable under 35 U.S.C. § 102(b), 35 U.S.C. § 103(a), or 35 U.S.C. §112. As a consequence, the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,



Harold C. Moore
Attorney for Applicants
Attorney Registration No. 37,892
Maginot Moore & Beck
Bank One Center Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115
Telephone: (317) 638-2922

CLAIM APPENDIX

1. (Amended) An arrangement for generating and storing metering information in a meter for measuring a consumed commodity, the arrangement including:

a) a processing circuit operable to receive commodity consumption information and generate metering information therefrom;

b) a non-volatile, rewriteable random access memory for storing the metering information during normal operation, the non-volatile, rewritable random access memory operable to retain the stored metering information in the absence of electrical power from a source external to the non-volatile, rewriteably random access memory.

2. (Original) The arrangement of claim 1 wherein the meter comprises an electricity meter and wherein:

the processing circuit is operable to generate load profiling information, said load profiling information including energy usage information for a plurality of time periods; and

wherein the non-volatile rewriteable random access memory is further operable to store the load profiling information.

3. (Original) The arrangement of claim 1 wherein the meter comprises an electricity meter and wherein:

the processing circuit is operable to generate metering information using one of a plurality of sets of meter formulae;

the non-volatile rewriteable random access memory is further operable to store the one of the plurality of sets of meter formulae.

4. (Original) The arrangement of claim 3 further comprising an external communication port and wherein the one of the plurality of sets of meter formulae stored in the non-volatile rewriteable random access memory may be replaced with a different one of the plurality of sets of meter formulae via communication with an external device through the external communication port.

5. (Original) The arrangement of claim 1 wherein the meter comprises an electricity meter and wherein:

the processing circuit is operable to generate metering information using a first set of calibration information; and

the non-volatile rewriteable random access memory is further operable to store the first set of calibration information.

6. (Original) The arrangement of claim 5 further comprising an external communication port and wherein the first set of calibration information may be replaced with a second set of calibration information via communication with an external device through the external communication port.

7. (Original) The arrangement of claim 1 wherein the non-volatile rewriteable random access memory is a ferromagnetic RAM.

8. (Original) The arrangement of claim 1 wherein the non-volatile rewriteable random access memory further stores at least one interim metering variable generated by the processing circuit and subsequently retrieved by the processing circuit for calculation of a metering value.

9. (Original) The arrangement of claim 1 wherein the non-volatile rewriteable random access memory further stores program code executed by the processing circuit.

10. (Original) The arrangement of claim 1 wherein:

the processing circuit is operable to generate statistical commodity consumption information, said statistical commodity consumption information including commodity usage information for a plurality of time periods; and

wherein the non-volatile rewriteable random access memory is further operable to store the statistical commodity consumption information.

11. (Original) The arrangement of claim 1 wherein the processing circuit includes plural processing devices, said plural processing devices including a digital signal processor.

20. (Amended) An arrangement for generating and storing metering information in an electricity meter for measuring consumed energy, the arrangement including:

a) a processing circuit operable to receive energy consumption information and generate metering information therefrom, said metering information including load profiling information;

b) a non-volatile, rewriteable random access memory for storing the metering information during normal operation, the non-volatile, rewritable random access memory operable to retain the stored metering information in the absence of electrical power from a source external to the non-volatile, rewriteably random access memory, said non-volatile, rewriteable random access memory further storing at least some program code executed by the processing circuit.

21. (Amended) An arrangement for generating and storing metering information in an electricity meter for measuring consumed energy, the arrangement including:

a) a processing circuit operable to receive energy consumption information and generate metering information using the received energy consumption information and a first set of calibration information;

b) a non-volatile, rewriteable random access memory for storing the first set of calibration information and for storing the metering information during

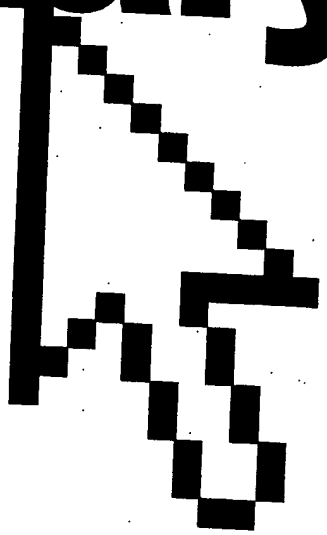
normal operation, the non-volatile, rewritable random access memory operable to retain the calibration information and the stored metering information in the absence of electrical power from a source external to the non-volatile, rewriteably random access memory.

EXHIBIT A

Microsoft® Press

Microsoft® Computer Dictionary

Fourth Edition



PUBLISHED BY
Microsoft Press
A Division of Microsoft Corporation
One Microsoft Way
Redmond, Washington 98052-6399

Copyright © 1999 by Microsoft Corporation

All rights reserved. No part of the contents of this book may be reproduced or transmitted in any form or by any means without the written permission of the publisher.

Library of Congress Cataloging-in-Publication Data
Microsoft Computer Dictionary. -- 4th ed.
p. cm.
Previous eds. published under title: Microsoft Press computer dictionary
ISBN 0-7356-0615-3
1. Computers Dictionaries. 2. Microcomputers Dictionaries.
I. Microsoft Press computer dictionary.
QA76.15.M538 1999
004'.03--dc21 99-20168
CIP

Printed and bound in the United States of America.

2 3 4 5 6 7 8 9 MLML 4 3 2 1 0 9

Distributed in Canada by Penguin Books Canada Limited.

A CIP catalogue record for this book is available from the British Library.

Microsoft Press books are available through booksellers and distributors worldwide. For further information about international editions, contact your local Microsoft Corporation office or contact Microsoft Press International directly at fax (425) 936-7329. Visit our Web site at mspress.microsoft.com.

Macintosh, Power Macintosh, QuickTime, and TrueType fonts are registered trademarks of Apple Computer, Inc. Kodak is a registered trademark of the Eastman Kodak Company. Intel is a registered trademark and Indeo is a trademark of Intel Corporation. Active Desktop, Active Directory, ActiveMovie, Active Platform, ActiveX, Authenticode, BackOffice, DirectInput, DirectX, Microsoft, Microsoft Press, MS-DOS, MSN, NetMeeting, NetShow, Visual Basic, Visual C++, Visual J++, WebTV, WebTV Network, Win32, Win32s, Windows, Windows NT, and XENIX are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries. PANTONE is a registered trademark of Pantone, Inc. Other product and company names mentioned herein may be the trademarks of their respective owners.

The example companies, organizations, products, people, and events depicted herein are fictitious. No association with any real company, organization, product, person, or event is intended or should be inferred.

Acquisitions Editor: Christey Bahn
Project Editor: Kim Fryer

F

flame[2] *vb.* **1.** To send an abusive or personally insulting e-mail message or newsgroup posting. **2.** To criticize personally by means of e-mail messages or newsgroup postings.

flame bait *n.* A posting to a mailing list, newsgroup, or other online conference that is likely to provoke flames, often because it expresses a controversial opinion on a highly emotional topic. *See also* flame[1], flame war. *Compare* troll.

flamefest *n.* A series of inflammatory messages or articles in a newsgroup or other online conference.

flamer *n.* A person who sends or posts abusive messages via e-mail, in newsgroups and other online forums, and in online chats. *See also* chat[1] (definition 1), newsgroup.

flame war *n.* A discussion in a mailing list, newsgroup, or other online conference that has turned into a protracted exchange of flames. *See also* flame[1].

Flash *n.* A vector graphics file format (extension .swf) developed by Macromedia to enable designers to add animation and interactivity to multimedia Web pages. Flash files can be played back with a downloadable Shockwave plug-in or a Java program. The file format has been released by Macromedia as an open standard for the Internet.

flash *vb. See* burn.

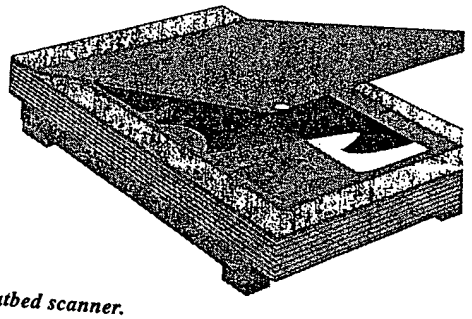
flash memory *n.* A type of nonvolatile memory. Flash memory is similar to EEPROM memory in function but it must be erased in blocks, whereas EEPROM can be erased one byte at a time. Because of its block-oriented nature, flash memory is commonly used as a supplement to or replacement for hard disks in portable computers. In this context, flash memory either is built into the unit or, more commonly, is available as a PC Card that can be plugged into a PCMCIA slot. A disadvantage of the block-oriented nature of flash memory is that it cannot be practically used as main memory (RAM) because a computer needs to be able to write to memory in single-byte increments. *See also* EEPROM, nonvolatile memory, PC Card, PCMCIA slot.

flash ROM \flash´ rom\ *n. See* flash memory.

flat address space *n.* An address space in which each location in memory is specified by a unique number. (Memory addresses start at 0 and increase sequentially by 1.) The Macintosh operating system, OS/2, and Windows NT use a flat address space. MS-DOS uses a segmented address space, in which a must be accessed with a segment number a set number. *See also* segmentation. *Compa* mented address space.

flatbed plotter *n.* A plotter in which paper i a flat platform and a pen moves along both traveling across the paper to draw an image. method is slightly more accurate than that u drum plotters, which move the paper under but requires more space. Flatbed plotters car accept a wider variety of media, such as vell acetate, because the material does not need t flexible. *See also* plotter. *Compare* drum plo pinch-roller plotter.

flatbed scanner *n.* A scanner with a flat trans surface that holds the image to be scanned, g a book or other paper document. A scan head the surface moves across the image. Some fla scanners can also reproduce transparent medi as slides. See the illustration. *Compare* drum handheld scanner, sheet-fed scanner.



Flatbed scanner.

flat file *n.* A file consisting of records of a single record type in which there is no embedded struc information that governs relationships between records.

flat-file database *n.* A database that takes the for a table, where only one table can be used for eac database. A flat-file database can only work with file at a time. *Compare* relational database.

flat file directory *n.* A directory that cannot conta subdirectories but simply contains a list of filena *Compare* hierarchical file system.

flat file system *n.* A filing system with no hierarch order in which no two files on a disk may have th same name, even if they exist in different director *Compare* hierarchical file system.